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DRAFT: DIAGNOSTIC/PROGNOSTIC EXPERIMENTS FOR CAPACITOR DEGRADATION AND HEALTH MONITORING IN DC-DC CONVERTERS

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ABSTRACT

Studying and analyzing the ageing mechanisms of electronic components avionics in systems such as the GPS and INAV are of critical importance. In DC-DC power converter systems electrolytic capacitors and MOSFET's have higher failure rates among the components. Degradation in the capacitors under varying operating conditions leads to high ripples output voltages and currents affecting downstream components leading to cascading faults. For example, in avionics systems where the power supply drives a GPS unit, ripple currents can cause glitches in the GPS position and velocity output, and this may cause errors in the Inertial Navigation (INAV) system, causing the aircraft to fly off course The work in this paper proposes a detail experimental and systematic study on analyzing the degradation phenomenon is electrolytic capacitors under high stress operating conditions. The output degradation is typically measured by an increase in ESR (Equivalent Series Resistance) and decrease in the capacitance value. . We present the details of our accelerated ageing methodology along with analysis and comparison of the results.

INTRODUCTION

In DC-DC converter power supply hardware electrolytic capacitors and MOSFET's have higher failure and degradation rates than other components in the systems. Variety of factors, such as High Voltage conditions, Operating Temperature, Transients, Reverse Bias, Strong Vibrations and high ripple current attribute to the failure in these components. These degraded units affect the performance and efficiency of the DC-DC converters in a significant way. Degradation and failures in the components occurs due to prolong operation periods under normal conditions or operations under extreme stress conditions like high temperature and high voltage. The paper develops a method for studying the degradation effects of electrolytic capacitors subjected to loading under extreme operating conditions i.e. high voltage stress and observe their impact on overall system performance.

The degradation in the DC-DC converters is typically measured by the increase in ESR (Equivalent Series Resistance) and decrease in capacitance value which leads to high ripple current and the drop in output voltage at the load. Typically the ripple current effects dominate, and they can have adverse effects on downstream components. The work in this paper is specifically directed towards DC-DC converters in Avionics systems. In these systems the power supply drives a GPS unit, and ripple currents at the converter output can cause glitches in the GPS position and velocity output, and this, in turn, may cause errors in the Inertial Navigation (INAV) system causing the aircraft to fly off course [1].

Switched-mode power supplies are widely used in DC-DC converters because of their high efficiency and compact size. DC-DC converters are important in portable electronic de-

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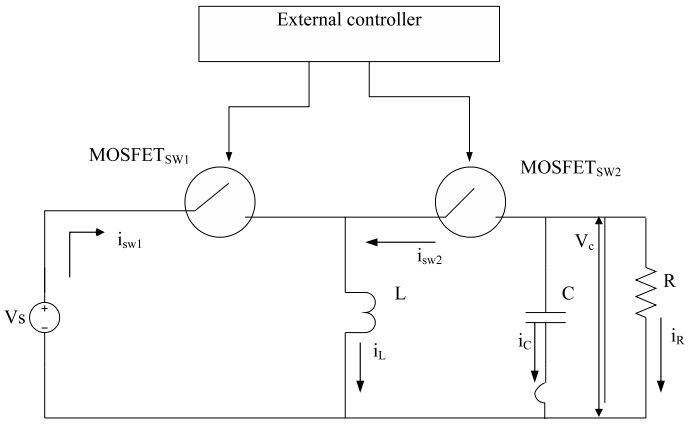

FIGURE 1. BUCK BOOST CONVERTER SCHEMATIC CIRCUIT

vices, which derive their power primarily from batteries. Such electronic devices often contain several sub-circuits with different voltage requirements (sometimes higher and sometimes lower than the supply voltage, and possibly even negative voltage). DC-DC converters can provide additional functionality for boosting the battery voltage as the battery charge declines. A typical buck-boost DC-DC converter schematic circuit is illustrated in Fig. 1.

In the literature it has been reported that electrolytic capacitors are the leading cause for breakdowns in power supply systems [2, 3]. The performance of the electrolytic capacitor is strongly affected by its operating conditions, which includes voltage, current, frequency, and working temperature. For degraded electrolytic capacitor the impedance path for the ac current in the output filter keeps increasing, thus introducing a ripple voltage on top of the desired DC voltage [4]. Continued degradation of the capacitor leads the converter output voltage to also drop below specifications and in some cases the combined effects of the voltage drop and the ripples may damage the converter itself in addition to affecting downstream components.

In general, capacitor degradation has been studied under nominal conditions as well as under extreme stress conditions, such as high voltage, high ripple, and adverse thermal conditions [5, 6]. Our overall goal in this work is to perform a systematic study of capacitor degradation stress conditions by replicating and extending some of the experimental studies that have been carried out in the past. Our approach is to perform empirical studies and then link them to theoretically-derived physics of failure models. This paper presents a first step by systematically collecting accelerated capacitor degradation data at high voltage operation. The results are observed, analyzed and are further compared with data observed from degradation under normal operating conditions. We also discuss and present our preliminary work for capacitance degradation in this paper as a first step to studying capacitance degradation using physics of failure models. The experimental studies, conducted at the NASA Ames Prognostics Centre of Excellence Lab, are discussed in greater detail along with observed result analysis later in the paper.

The rest of this paper is organized as follows. The the following section discusses the mechanisms for capacitor degradation in DC-DC converters. The next section discusses accelerated degradation experiments conducted on electrolytic capacitors under high voltage stress . The following sections discusses the analysis methods and comparison of accelerated degradation with normal degradation. The paper concludes with discussion of the results and future work.

ELECTROLYTIC CAPACITOR DEGRADATION

This section discusses in detail the conditions under which the capacitor degrades leading to faults in the system. We study the adverse effects of the load conditions, operating conditions, ripple currents, which cause degradation by raising the temperatures in the capacitor core.

Physical Model of the Capacitor

An aluminum electrolytic capacitor, illustrated in Fig. 2 consists of a cathode aluminum foil, electrolytic paper, electrolyte, and an aluminum oxide layer on the anode foil surface, which acts as the dielectric. When in contact with the electrolyte, the oxide layer possesses an excellent forward direction insulation property [7]. Together with magnified effective surface area attained by etching the foil, a high capacitance is obtained in a small volume [8].

Since the oxide layer has rectifying properties, a capacitor has polarity. If both the anode and cathode foils have an oxide layer, the capacitors would be bipolar [9]. In this paper, we analyze the "non-solid" aluminum electrolytic capacitors in which the electrolytic paper is impregnated with liquid electrolyte. There is another type of aluminum electrolytic capacitor, that uses solid electrolyte but we will not include these types of capacitors in this discussion [10].

Degradation Mechanisms

There are several factors that cause degradation in electrolytic capacitors. As the degradation increases time the component fails , and this impacts the overall system functionality. The definition of failure and some of the failure modes are discussed below. Failures in a capacitor can be one of two types: (1) catastrophic failures, where there is complete loss of functionality due to a short or open circuit, and (2) degradation failures, where there is gradual deterioration of capacitor function. Degradations are linked to an increase in the equivalent series resistance (ESR) and decrease in capacitance over time [11, 12]. Capacitor degradation is typically attributed to:

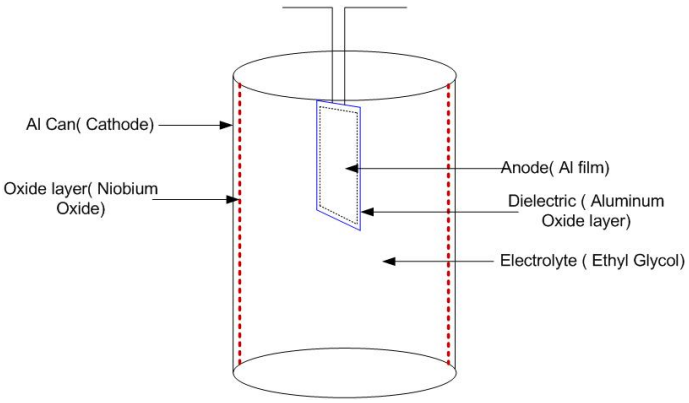

FIGURE 2. PHYSICAL MODEL OF ELECTROLYTIC CAPACITOR

1. High Voltage conditions: The capacitance decreases and ESR increases.
2. Transients: The leakage current can be high and an internal short-circuits can occur.
3. Reverse Bias: The leakage current becomes high with loss of capacitance and increase in ESR.
4. Strong Vibrations: These can cause internal short circuits, capacitance losses, high leakage currents, increase in ESR and open circuits.
5. High Ripple current: These cause internal heating, increasing the core temperature which results in gradual aging of the capacitor.

A primary reason for wear out in aluminum electrolytic capacitors is due to vaporization of electrolyte, which, in turn leads to a drift in the main electrical parameters of the capacitor. One of the primary parameters is the equivalent series resistance (ESR). The ESR of the capacitor is the sum of the resistance due to aluminum oxide, electrolyte, spacer, and electrodes (foil, tabbing, leads, and ohmic contacts) [6, 7]. The health of the capacitor is often measured by the ESR value. Over the operating period, the capacitor degrades, i.e., its capacitance decreases and ESR increases. Considering the current ESR value and operating conditions the remaining useful life of the capacitor can be calculated using model-based methods. There are certain industry standards for these parameter values, if the measurements exceed these standards then the component is considered failed, i.e., the component has reached its end of life, and should be immediately replaced before further operations [2, 13, 14]. The next section discusses in detail the experiments being conducted on the DC-DC converter hardware to study and measure the degradation the relevant capacitor parameters.

CAPACITOR DEGRADATION EXPERIMENTS

To observe the degradation phenomenon we carried out experiments with a set of capacitors. This experiment was conducted to determine degradation in the capacitors under high voltage operation and working at room temperature. The output filter capacitor in a DC-DC converter is the component under study for degradation experiment. The capacitor connections lead are made available such that measurements can be taken easily without any noise in the measurements and without disturbing the rest of the system setup.

Experiment: Accelerated Degradation

For this experiment six sets of electrolytic capacitor components were considered. Electrolytic capacitors of 2200μF capacitance, with a maximum rated voltage of 10V, maximum current rating of 1A and maximum operating temperature of 85°C was used for the study. This was the suggested type of capacitor by the manufacturer of the hardware for DC-DC converters. The capacitors used for the experiments were picked from the same lot of one manufacturer, and all the capacitors in the lot had similar specifications. The electrolytic capacitors under test were measured for the initial ESR and capacitance value with other related measurement details before the start of the experiment at room temperature.

The ESR and capacitance values were measured using an SP-150 Biologic SAS measuring instrument. The average initial ESR value was measured to be around 0.056mΩ and average capacitance of 2123μF for the set of capacitors under test. The degrading electrolytic capacitor is modeled as a series RC circuit. The ESR value is real impedance measured through the terminal software of the instrument. Similarly the capacitance value is computed from the imaginary impedance using Electrochemical Impedance Spectroscopy Z-Fit. The details of the method are in [15, 16]. These values can be calculated directly at the time of measurement or later off-line.

Since we were studying the effect of high voltage on degradation of the capacitors, no DC-DC converter hardware was used, only the capacitors were subjected to high voltage stress through an external supply source. A constant voltage source with a square wave of 2 Hz frequency and 5V output was used for generating the required signal. The output voltage from the source was then ramped upto the required voltage of 13.5V using an external hardware circuit. This ramped up voltage was selected to be higher than the rated voltage of 10V to observe accelerated degradation in the capacitor. The 2 Hz square wave frequency output subjects the capacitor to a continuous charge/discharge cycle. A load of 100Ω was connected at capacitor terminal to discharge the capacitor completely within the

FIGURE 3. INPUT AND OUTPUT SIGNALS ON THE OSCILLOSCOPE

specified cycle time. A digital oscilloscope was used to monitor the input and output voltage signals continuously. A snap shot of the input and the output voltage signals is shown in Fig. 3

The measurements were recorded approximately at every 8-10 hours of the total 150 plus hours of operation time. As the capacitors were subjected to high voltage stress above the rated voltage, readings were taken at very short intervals of time to capture the rapid degradation phenomenon in the ESR and capacitance values. The ambient temperature for the experiment was controlled and kept at 25°C . During each measurement the voltage source was shut down, the capacitors were discharged completely and then measurements for the ESR and capacitance were taken. This was done for all the six capacitors under test. Keeping all the conditions intact the experiment was started again till the next measurement. This procedure was followed and recorded for all the readings taken during the time of the experiment.

DATA ANALYSIS

All the data collected was analyzed to observe how the ESR and the capacitance were changing over the period of time. As per the industry standards, capacitors are considered completely degraded and not usable in the circuit when it's ESR value reaches 2.8 times of the initial ESR value measured. In case of capacitance the value should not go below 20% of the initial value after which the capacitor is considered to be not healthy to be used in the circuit.Our goal is to continue the experiment to capacitor failure, but for this work we did not run the experiments till the failure of the component.

From the collected data over the period of time we can then interpolate the remaining healthy life of the capacitor. Thus with this data we predict approximately the capacitor degradation rates, and the time to failure under high stress operating conditions.

TABLE 1. ESR PERCENTAGE AND VALUE INCREASE DUE TO DEGRADATION

Time (Hours)	Value(mΩ)	% Increase
0	0.0557	0
20	0.0567	9.48
40	0.0606	17.04
60	0.0646	24.86
80	0.0673	30.06
100	0.0693	33.91
120	0.0717	38.45
140	0.0739	42.76
160	0.0776	49.91

ESR Data Analysis

Table 1 shows the average ESR increase in percentage and value respectively over the period of operation. Since all the capacitors were subjected to similar conditions of temperature, input voltage and load, we averaged the collected data and the table discusses the same. *(Please note the values have been truncated just for the tables, but actual values have been used during the calculations and plotting of the data.)*

Fig. 4 shows the plot for the average increase in the ESR values for all capacitor units for the experimental period. It is observed that initially during the first few hours of the experiment the increase is quite steady and then at around 30- 40 hours of operation there is a steep increase in the slope. At the end of 160 hours under high voltage stress the ESR value increase by almost 50% of the initial value.

This experimental work is still in the initial stages and we are collecting further degradation data, analysis and refining the experiments. With the current set of data collected a third and fourth order curve was fitted as shown in Fig. 4. It was observed that the fourth order curve fitted the data most appropriately from the least squares residuals. Equation 1 defines the approximate ESR degradation rate from which we can calculate the healthiness of the capacitor.

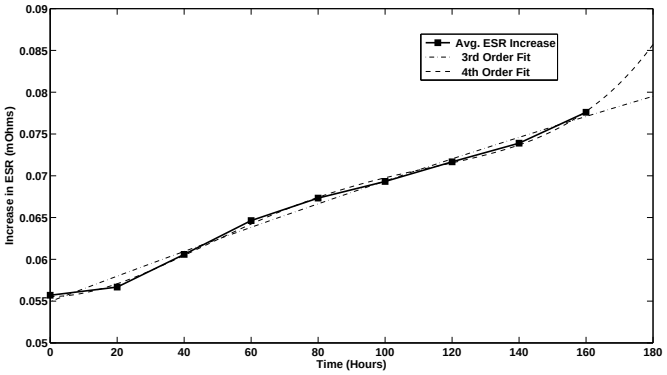

FIGURE 4. ESR INCREASE AND CURVE FITTING

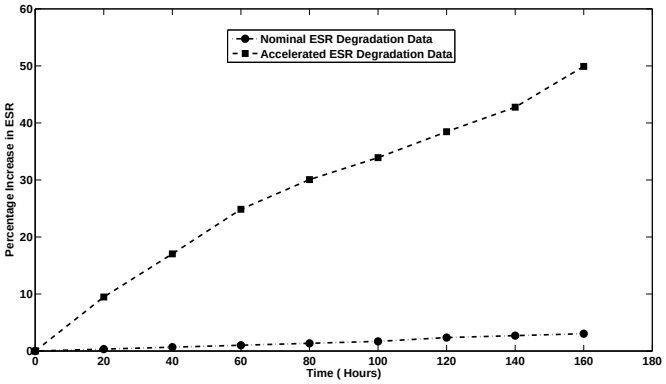

FIGURE 5. ESR COMPARISON : NORMAL AND ACCELERATED DEGRADATION

$$ESR_t = 0.0014 * [\frac{t-80}{55}]^4 - 1.7e-6 * [\frac{t-80}{55}]^3 - 0.0034 * [\frac{t-80}{55}]^2 + 0.0076 * [\frac{t-80}{55}] + 0.0067 \quad (1)$$

where :

t = Time in Hours.

To study this rapid degradation we compared the accelerated degradation data with normal degradation data for the same period of experimental time. In the normal condition of operation the capacitor was connected to the DC-DC converter hardware unit with a 5V output voltage at room temperature. This experiment was carried out to study the degradation of capacitors for prolonged period of almost 3000 plus hours of operating time. The details of the experiments conducted and the analysis for normal degradation in electrolytic capacitors is described in [17]. Fig. 5 shows increase in ESR value by 2 - 2.5% for normal operation whereas in the case of high voltage stress operation the ESR increased by almost 50% of the initial value. Thus we observe that different operating conditons have a significant impact on the healthiness of the components.

Capacitance Data Analysis

Table 2 shows the average percentage decrease in the values of the capacitance over the period of operation. The table shows the decrease in the capacitance over 20 hour interval for 160 hours of operation. *(Please note the values have been truncated just for the tables, but actual values have been used during the calculations and plotting of the data.)*

Fig. 6 shows the plot for the average capacitance of all the six capacitors. With reference to the average capacitance data a quadratic fit (second order) and cubic fit (third order) was done for the data. From the collected data over the period of time

TABLE 2. CAPACITANCE PERCENTAGE AND VALUE DECREASE DUE TO DEGRADATION

Time (Hours)	Value (μF)	% Decrease
0	2123	0
20	2110	0.6089
40	2089	1.565
60	2078	2.053
80	2048	3.528
100	1995	5.998
120	1943	8.462
140	1892	10.86
160	1833	13.64

we can then interpolate the remaining useful life of the capacitor under high stress operating conditions. Thus with this data we can approximately predict the capacitor degradation rate, and hence the time to failure. From the least squares calculation if was found that the quadratic fit matched the experimental data in the best manner. The equation for the degradation data approximation is given as below.

$$Capacitance_t = -4.1e-5 * [\frac{t-90}{61}]^2 - 1.3e-4 * [\frac{t-90}{61}] + 0.002 \quad (2)$$

where :

t = Time in Hours.

Similar to the ESR degradation comparison discussed above,

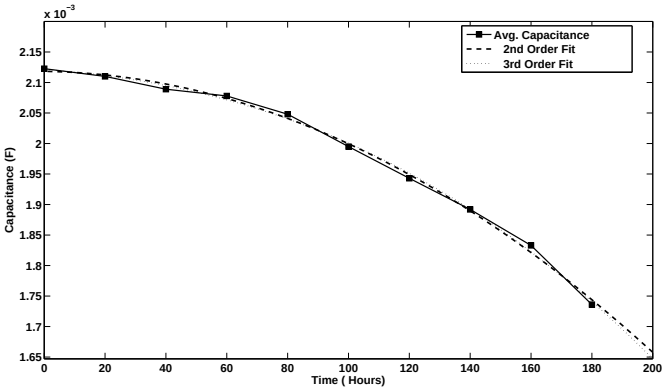

FIGURE 6. CAPACITANCE DECREASE AND CURVE FITTING

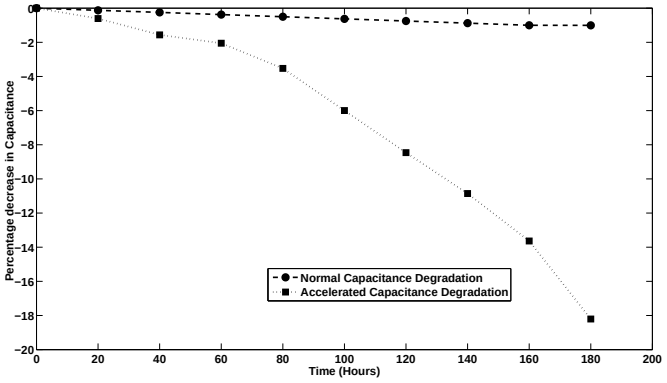

FIGURE 7. CAPACITANCE COMPARISON : NORMAL AND ACCELERATED DEGRADATION

a comparison for the decrease in the capacitance under high stress operation and normal operation was done. Fig. 7 shows the comparison between the decrease in capacitance for the two operating conditions. Under normal operating conditions the capacitance decreased by less than 1% [17] while under high voltage stress condition for the same period of time the capacitance decrease by almost 13% which is a significant decrease in the value. This shows that high electrical stress accelerates the degradation phenomenon in electrolytic capacitors. This degradation can be related to the physics of failure of the component. This was the preliminary work done to look at the effects of different operating conditions on components. Our future goal is to observe this degradation at different voltages and model the complete physics of failure phenomenon.

CONCLUSION AND FUTURE WORK

In this work we have discussed the importance of studying degradation in the components of a system. Specially in case of electrolytic capacitors which are the most important components in a DC-DC converter sub-system. As discussed different operating conditions can degrade the component in different ways and through this systematic study our aim to develop a combined failure model of capacitor degradation for different operating conditions. In our previous work we studied normal degradation of capacitors, this work included accelerated degradation under high voltage stress. We further will be studying more voltage related degradation and also the effect of temperature stress. This combined work will give us an approximate prognostic prediction on the behavior and health monitoring of the component. These combined degradation models can then be used to study their cascading effect on the avionics subsystems like GPS and INAV.

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