Towards Accelerated Aging Methodologies and Health Management of Power MOSFETs (Technical Brief)

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ABSTRACT

Understanding aging mechanisms of electronic components is of extreme importance in the aerospace domain where they are part of numerous critical subsystems including avionics. In particular, power MOSFETs are of special interest as they are involved in high voltage switching circuits such as drivers for electrical motors. With increased use of electronics in aircraft control, it becomes more important to understand the degradation of these components in aircraft specific environments. In this paper, we present an accelerated aging methodology for power MOSFETs that subject the devices to indirect thermal overstress during high voltage switching. During this accelerated aging process, two major modes of failure were observed – latch-up and die attach degradation. In this paper we present the details of our aging methodology along with details of experiments and analysis of the results.*

1. INTRODUCTION

The aging of electronics and the associated unexpected failures are a major concern in the aerospace industry where these devices serve as critical components in various subsystems. Understanding the aging mechanisms of electronic components and predicting impending failures is a challenging problem. Among other electronic components used in avionics, power electronics components are of particular importance for subsystems like controls, communications, navigation, and radar systems where they are extensively used for high voltage switching.

Electronic components in avionic systems are often subjected to off-normal behavior. For instance power MOSFETs can encounter high-voltage operations quite frequently, with these high voltages creating large electric fields internally that can cause rapid degradation of the devices. In order to develop health management technologies for such devices, it is important to understand the physical behavior due to device aging and the root causes for these failures. In the research phase, a variety of sensor measurements with high sampling frequency are needed to observe any noticeable changes due to aging or other associated failure mechanisms. Based on a detailed study of device functioning, one needs to identify a set of useful measurements that can lead to development of precursors to failure(s). In absence of such data from real applications, conducting controlled but accelerated laboratory experiments that would then be used to characterize fault evolution dynamics and to consequently develop a fault growth model would be

ideal. An approximate fault growth model along with relevant sensor measurements have been shown to develop effective prognostics algorithms (Saha et al. 2009). In this paper we present our efforts towards conducting and analyzing accelerated aging of an important class of electronic components called power MOSFETs.

The accelerated aging experiments in this study were conducted using a test platform that involved repeated indirect thermal overstress of the devices through high power switching until device failure. The test platform allows for monitoring of various external parameters such as drain current, drain to source voltage, gate voltage, and package temperature during ON and OFF duty cycle. The trends of variation in these externally observable parameters are then analyzed in order to relate them to the physical phenomena that might be potentially contributing to aging and the subsequent failures within the device.

The remaining sections of this paper, 2 through 6 are organized as follows. In section 2, related work in the field of power electronics aging and reliability is presented. Section 3 provides a detailed description of our accelerated aging setup. Section 4 includes description of our experiments and the aging methodology. Results obtained and analysis constitutes section 5, followed by some discussions in section 6.

2. REVIEW OF POWER MOSFET AGING APPROACHES

Based on the application domain, several aging approaches have been employed to evaluate power MOSFET reliability. One of the methods involved electrical pulsing of power MOSFETs under controlled temperatures to cause electro-thermal fatigue (Khong et al. 2007). The aging conditions used in the experiments simulated stresses experienced by automotive components (Khong et al. 2005). This aging was performed with a duty cycle of 5-10% and with current stresses measuring 120A. These aging stresses led to a high drain-source ON-resistance increase of the power MOSFET that was shown to be a result of die attach de-lamination and bond-wire cracking at the source terminal.

In (Dupont et al. 2007), the authors performed a reliability assessment of power MOSFETs under high temperatures. These devices were power cycled with a duty cycle of 30% and drain current of 150A. The maximum junction temperature was reported to be near 175ºC. When the change in junction temperature (ΔT_j) was high, high drain to source leakage current was observed. When the ΔT_j was low, high on-resistance was reported that was found to be a result of bond wire cracking.

Another aging methodology considered the effect of radiation on power MOSFET reliability (Wahle et al. 1990). In this study, power MOSFETs were exposed to low dosage rates (1.0 krad(Si)/day) as well as high dosage rates (3.3 rad(Si)/s). These exposures were carried out with the transistors at a constant as well as a time varying gate bias. The results of these tests showed reduced threshold voltage and reduced mobility as a result of oxide trapped charge and interface charges. In another study on the effects of high gate bias stress, it was shown that with gate voltages ranging from 88 V to 94 V and the drain source grounded for 2 hours, this resulted in the lowering of threshold voltage and mobility reduction (Stojadinovic et al. 2005).

3. ACCELERATED AGING TESTBED SETUP

In this section, we present details about our accelerated aging test bed for power MOSFETs. For a clearer understanding of the aging setup, we first present some background information of the devices being tested including operational details and failure modes. Our aging mechanism involves aging through indirect temperature overstress, thus the device is cycled through phases of rapid switching at high voltages and no switching. No heat sink is employed in these experiments, which results in excessive heating of the device causing accelerated thermal degradation.

3.1 Background

Power MOSFETs were first developed in the 1970s and soon replaced power bipolar junction transistors (BJT's). These devices are voltage controlled unlike power BJTs that are current controlled, and hence require a less complicated gate driver circuit. Continued research and development in device design and fabrication processes have led to improvements in power MOSFET performance. Today, it is possible to fabricate MOSFETs with breakdown voltages as high as 600V accompanied by a low ON-resistance of 80mΩ. Reduced switching and conduction losses in these devices have led to improved performance of switch mode power supplies and automotive electronics. Power MOSFETs today are the devices of choice for high frequency applications (up to few hundreds of MHz) and voltages below 200V.

The schematic of the power MOSFET used in this study is shown in Figure 1. This HEXFET structure from International Rectifier has an array of hexagonal cells. A positive bias on the gate above the threshold voltage leads to formation of a conductive channel below the gate oxide. A positive bias on the drain leads to transistor current flow through the conductive channel. When the source-drain terminals are reverse

biased, the current flows through the integral body diode labeled as diode current in Figure 1.

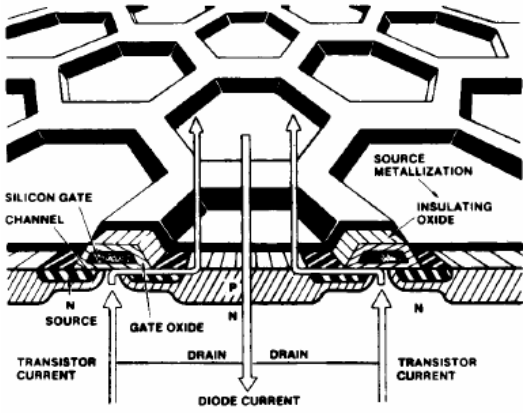

Figure 1. HEXFET power MOSFET structure from (Haran et al. 2007).

3.2 Power MOSFET Failure Mechanisms

Failures in power MOSFETs typically occur as a result of the activation of the parasitic BJT inherent to the power MOSFET structure (Blackburn 1987). Activation of this parasitic BJT results in loss of gate control which ultimately leads to device dysfunction. Several failure mechanisms reported in the literature are related to parasitic BJT activation depending on different load conditions. These failure mechanisms include a high rate of change of the drain source voltage (dV_{DS}/dt) (Kuo et al. 1983; Singh 2004), reverse recovery of the body diode (Busatto et al. 1997) and single event burnouts as a result of ion hits (Haran et al. 2007).

The most prominent failure mode observed in our experiments so far involved loss of gate control at turn-off. The loss of gate control is preceded by a sudden drop in on-resistance after it gradually increases for a long time during aging. Initially the on-resistance increases due to device heating caused by the aging process. The sudden drop indicates the activation of the parasitic BJT resulting in loss of gate control. Since the BJT gets activated during turn-off, the failure is possibly caused by high leakage currents flowing through the body diode.

During turn-off, current reversal takes place across the body diode as it is now forward biased. This current flow through the integral body diode is called reverse recovery current (I_{RR}). With an increase in device temperature, the reverse recovery current increases. Additionally, the resistance of the p-body region ($R_{p\text{-}body}$) increases with temperature increase. When the reverse recovery current and the body region resistance are large enough to cause a sufficient potential drop to turn-on the BJT, gate control is lost as a consequence of device current flowing directly from drain to source without traveling through the inversion layer. This phenomenon is illustrated in Figure 2.

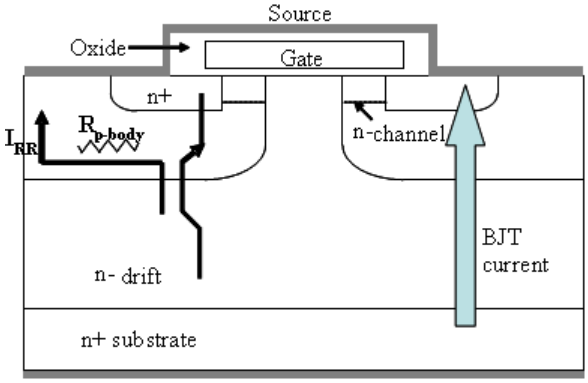

Figure 2. BJT activation due to diode reverse recovery current.

3.3 Accelerated Aging Setup

Of the various aging mechanisms, thermal and electrical overstresses are the most common suspects. Thermal cycling and chronic temperature overstress lead to thermal stresses in electronics. Hence thermal cycling is among the most prevalent accelerated aging methodologies for electronics. Thermal cycling subjects devices to rapid changes in temperature causing thermal expansions and contractions. In our aging setup, we use indirect thermal cycling for accelerated aging of power MOSFETs. The thermal changes are the result of the applied electrical power given that no additional external heat sink is used during the aging process. Figure 3 shows a high-level schematic of our aging test bed.

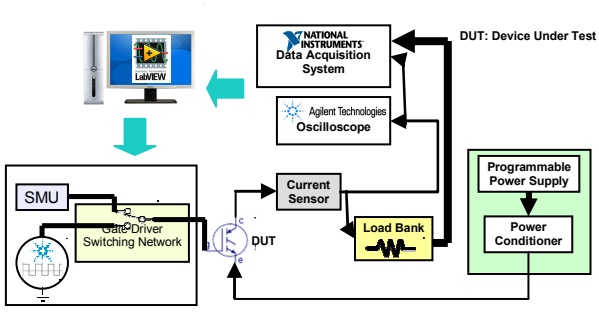

Figure 3. High-level schematic of experiment test bed for aging via thermal cycling.

Switching of the device is controlled by setting temperature limits. When the temperature falls below a certain level T_{min}, the device is turned to switching mode. When temperature rises beyond a maximum limit T_{max}., the gate voltage is set to zero volts and does not perform any switching. During the switching mode, a switching control square waveform with 40% duty

cycle, 1 kHz frequency and 12V amplitude is applied at the gate causing the device to switch rapidly. This generates a large amount of power, resulting in excessive heating of the device in the absence of a heat sink. When the temperature rises beyond a pre-set level T_{max}, the device is set back to the no-switching state. Additionally, a higher temperature threshold $T_{thresold}$ is used to stop the test when the device enters *thermal runaway*. In this case, the device is switched off completely (gate and drain-source voltages set to zero) in order to avoid catastrophic damages. The temperature is monitored using an infra-red sensor. The actual setup is shown in Figure 4. The complete setup is controlled using a LabView (National Instruments) interface that includes instrument control as well as data collection modules. Further details of the test board can be found in (Sonnenfeld et al. 2008).

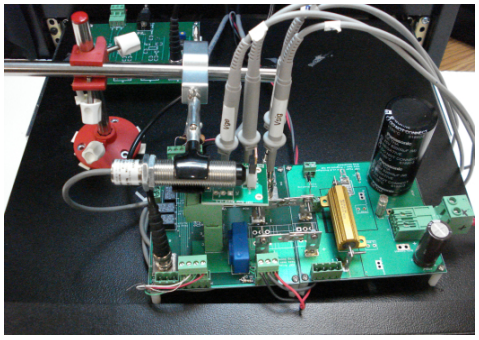

Figure 4. Test board for experiments with thermal cycling.

4. AGING METHODOLOGY

Two aging methodologies for power MOSFETs were explored in this study. The first method involved aging the devices by exposing them to thermal overstress with a constant load profile. The objective was to determine the failure modes, mechanisms and precursors to failure when these devices were operated in extreme temperatures well beyond the safe operating area. The package temperature profile for one of the devices aged by constant temperature load is shown in Figure 5. The package temperature was maintained at 230°C for the duration of the test. The failure mode observed was an increase in package temperature indicating the onset of thermal runaway. It took 35 minutes for device failure to occur.

The cause for thermal runaway was determined to be device latch-up. Latch-up is a condition in which the device can no longer be controlled by the gate voltage. In Figure 6, we observe that the drain current increased from 3 A to 15 A, failing to turn-off when gate voltage is reduced to zero. This is evidence of loss of gate control that leads to rapid temperature build up within the device.

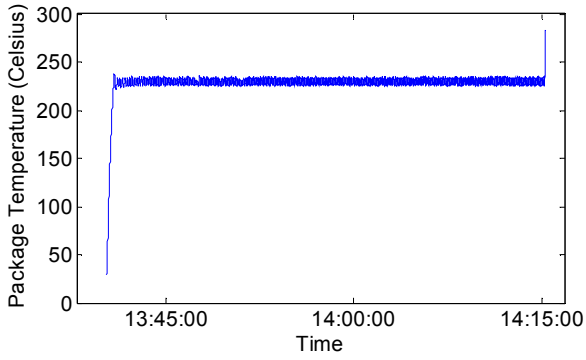

Figure 5. Package temperature evolution with aging time.

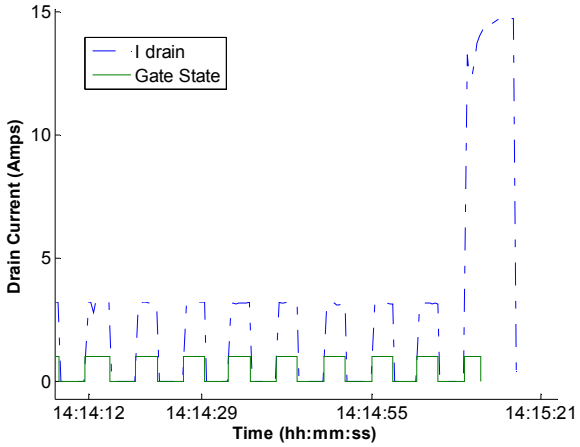

Figure 6. Latch-up failure of the power MOSFET.

The ON resistance of the device ($R_{DS(ON)}$) displayed a sudden drop at the onset of failure after a gradual rise (Figure 7). The rise of the resistance with time is evidence of gradual degradation in the device. The sudden drop in resistance at the onset of latch up indicates the activation of the parasitic BJT.

In the second aging method, a stepped temperature load profile was used to age the devices. The stepped profile was used to enable a better understanding of device degradation in the safe operating area and to allow measurements of DC characteristics such as breakdown voltage and threshold voltage periodically during the aging process. The load profile used in this study is shown in Figure 8. Device failure occurred after three cycles. The failure mode was failure to switch as a result of the increased resistance of the device. Each cycle was of ~50 minutes duration and the device failed in 2.5 hours.

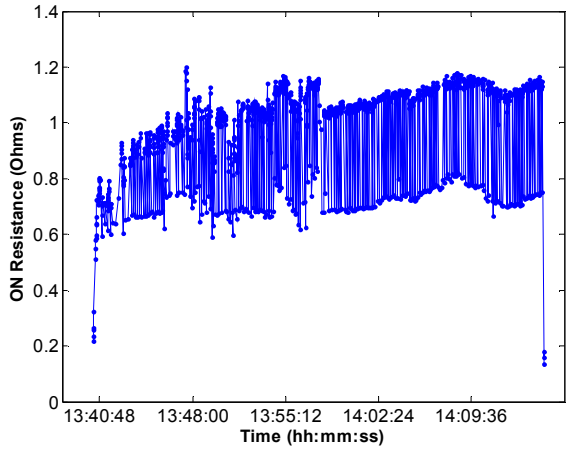

Figure 7. Power MOSFET resistance profile with time.

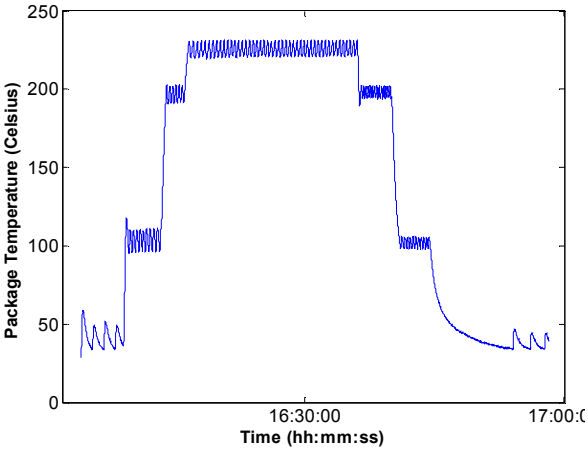

Figure 8. Stepped load temperature profile.

The failure occurred during the cool down period from 200°C to 100°C. The load profile at failure is shown in Figure 9. The failure occurred as a result of increased resistance in the device. As a result of the increased resistance, the drain current dropped and the transistor failed to switch.

The drain current reduction is shown in Figure 10, it is a response obtained during a gate pulse of 12V. The drain current responses to the input gate pulse in are obtained while at 100°C. These gate pulses were applied to the device at periodic intervals during the aging. Please note that the time in the x-axis is not the aging time but the period of the input gate pulse which is 1ms with each data point representing 20µs. To identify the primary failure mechanism in operation, electrical characterization data was analyzed and physical degradation analysis was performed.

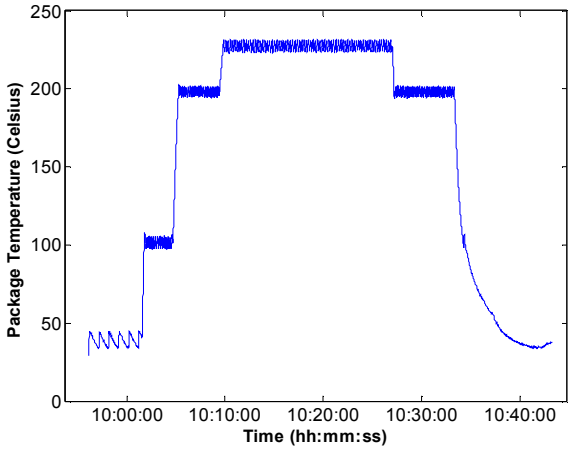

Figure 9. Temperature profile at failure.

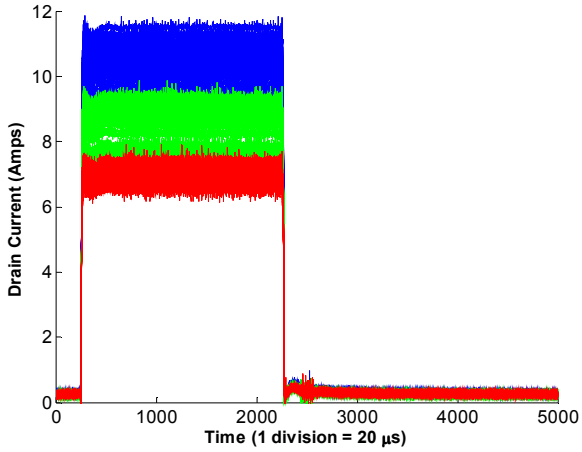

Figure 10. Drain current at failure.

5. ELECTRICAL CHARACTERIZATION AND PHYSICAL DEGRADATION ANALYSIS

The threshold voltage of the device is the voltage at which the device drain current begins to flow. The threshold voltage is an indicator of the health of the oxide. Degradation in the oxide in the form of positive trapped charges causes the threshold voltage to decrease whereas negative trapped charges increase the threshold voltage. The threshold voltage measured for the first cycle is compared with the threshold voltage in the final cycle. The threshold voltage shows no change as seen in Figure 11 indicating that there is no damage to the gate oxide.

The breakdown voltage measurements are shown for each of the three cycles in Figure 12. The breakdown voltage is an indicator of the ability of the device to block drain source voltage when there is no voltage applied to the gate. The changes in breakdown voltage are a function of the integrity of the body diode.

Degradation in the body diode results in lowering of the breakdown voltage. As seen in Figure 12, no significant breakdown voltage degradation was observed during the aging process. The small differences in the values observed are within the measurement tolerances for the equipment.

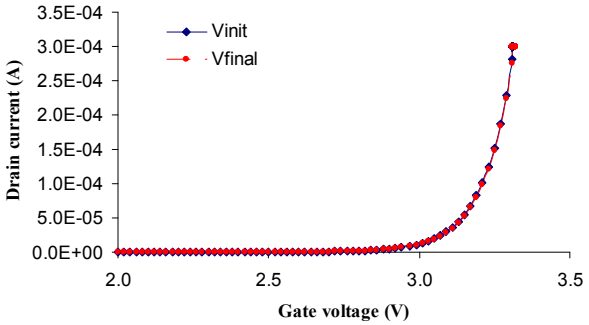

Figure 11. Threshold voltage comparison between first and third aging cycle.

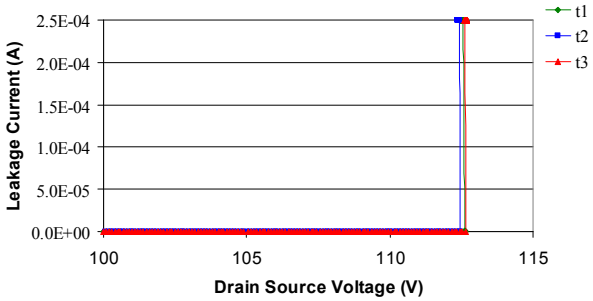

Figure 12. Breakdown voltage comparison for the three aging cycles.

Physical degradation analysis was performed on the aged devices using a scanning acoustic microscope. A 50 MHz transducer was used to generate acoustic signals and the analysis was performed with the heat sink facing the transducer. The die attach, which is the interface between the silicon die and copper heat sink was imaged. The die attach was observed to be degraded as seen in Figure 13. The image on the left in Figure 13 is at the interface between the heat sink and the die attach. The image on the right is obtained at a greater depth within the die attach layer. The bright areas in the lower portion of the die attach indicate the presence of voids and/or de-lamination. The hypothesis for the failure observed is that the die attach voiding and/or de-lamination occurred during the cooling period of the aging profile leading to a large rise in resistance as seen by the observed drop in drain current at failure.

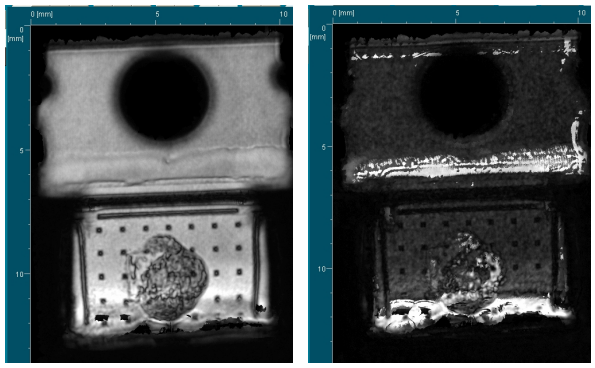

Figure 13. CSAM analysis of the power MOSFET.

6. DISCUSSION

Latch up failures of power MOSFETs typically occur as a result of the activation of the parasitic BJT inherent in the power MOSFET structure (Blackburn 1987) as shown in Figure 14. Activation of this parasitic BJT results in loss of gate control which ultimately leads to device destruction. Several failure mechanisms have been reported to result in parasitic BJT activation depending on load conditions. These failure mechanisms include high rate of change of the drain source voltage (dV_{DS}/dt) (Kuo et al. 1983; Singh 2004), reverse recovery of the body diode (Busatto et al. 1997) and single event burnouts as a result of ion hits (Haran et al. 2007)

One Power MOSFET failure mode observed in the aging experiments was loss of gate control at turn-off. The loss of gate control was preceded by a sudden drop of on-resistance after a gradual increase as seen in Figure 7. The initial increase in on-resistance is due to device heating caused by the aging process. The sudden drop indicates activation of the parasitic BJT resulting in loss of gate control. The high temperature aging leads to high leakage currents through the body diode and increased resistance of the p-body region. This high leakage current and body resistance may have caused a sufficient voltage drop to turn-on the parasitic BJT. With the activation of the BJT, the current path is directly from drain to source without traveling through the inversion layer as shown in Figure 14.

The total on-resistance (RDS(on)) of the power MOSFET is the sum of several resistance components that include source contact resistance (Rsc), source resistance (Rn+), channel resistance (Rch), accumulation resistance (Racc), junction field effect transistor (JFET) resistance (RJFET), drift resistance (Rdrift), substrate resistance (Rsub), and drain contact resistance (Rdc) (Baliga 2008). The total on-resistance increases with an increase in temperature as a result of mobility (μ) reduction of the charge carriers. This mobility reduction is attributed to increased scattering of charge carriers with temperature. The decrease in

mobility with temperature is based on the material properties and doping levels of the semiconductor (Baliga 2008). In the aging experiments, one additional failure mode observed was the failure of the transistor to switch due to the increase in the on-resistance of the device. The root cause of increased device temperature is due to the degradation in the die attach as observed from the CSAM results and which has been previously observed with this aging platform (Patil et al. 2009).

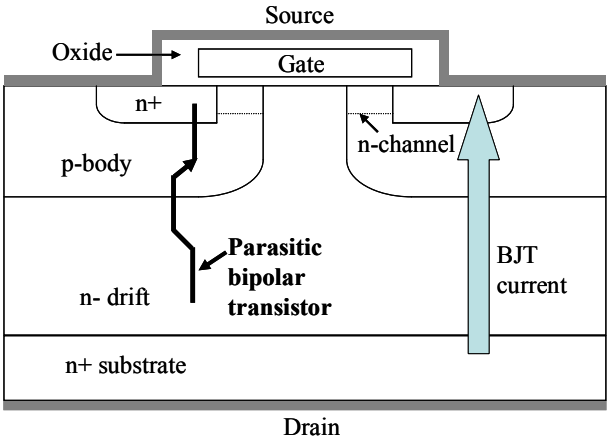

Figure 14. BJT activation leading to loss of gate control

Future work would involve more accelerated aging testing in order to demonstrate repeatability of the experiments. Also, failure analysis will be performed to develop further insight into the underlying failure mechanisms.

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BIOGRAPHIES

Jose R. Celaya is a research scientist with Stinger Ghaffarian Technologies at the Prognostics Center of Excellence, NASA Ames Research Center. He received a Ph.D. degree in Decision Sciences and Engineering Systems in 2008, a M. E. degree in Operations Research and Statistics in 2008, a M. S. degree in Electrical Engineering in 2003, all from Rensselaer Polytechnic Institute, Troy New York; and a B.S. in Cybernetics Engineering in 2001 from CETYS University, Mexico.

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Phil Wysocki has extensive knowledge and background in test model based data acquisition, as well as programming and system design for diagnostics. He has developed and implemented test design for aging and characterizing IC's and environmental testing. This includes optimization of test hardware and software for prognostics. Phil earned a Bachelor of Science Degree in Computer Science along with over 25 years experience demonstrated at NASA Ames Research Center.

Kai Goebel received the degree of Diplom-Ingenieur from the Technische Universität München, Germany in 1990. He received the M.S. and Ph.D. from the University of California at Berkeley in 1993 and 1996, respectively. Dr. Goebel is a senior scientist at NASA Ames Research Center where he leads the Diagnostics & Prognostics groups in the Intelligent Systems division. In addition, he directs the Prognostics Center of Excellence and he is the Associate Principal Investigator for Prognostics of NASA's Integrated Vehicle Health Management Program. He worked at General Electric's Corporate Research Center in Niskayuna, NY from 1997 to 2006 as a senior research scientist. He has carried out applied research in the areas of artificial intelligence, soft computing, and information fusion. His research interest lies in advancing these techniques for real time monitoring, diagnostics, and prognostics. He holds eleven patents and has published more than 100 papers in the area of systems health management.