Precursor Parameter Identification for Insulated Gate Bipolar Transistor (IGBT) Prognostics

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***Abstract*—Precursor parameters have been identified to enable development of a prognostic approach for insulated gate bipolar transistors (IGBT). The IGBT were subjected to thermal overstress tests using a transistor test board until device latch-up. The collector-emitter current, transistor case temperature, transient and steady state gate voltages, and transient and steady state collector-emitter voltages were monitored in-situ during the test. Pre- and post-aging characterization tests were performed on the IGBT. The aged parts were observed to have shifts in capacitance-voltage (C-V) measurements as a result of trapped charge in the gate oxide. The collector-emitter ON voltage $V_{CE(ON)}$ showed a reduction with aging. The reduction in the $V_{CE(ON)}$ was found to be correlated to die attach degradation, as observed by scanning acoustic microscopy (SAM) analysis. The collector-emitter voltage, and transistor turn-off time were observed to be precursor parameters to latch-up. The monitoring of these precursor parameters will enable the development of a prognostic methodology for IGBT failure. The prognostic methodology will involve trending precursor data, and using physics of failure models for prediction of the remaining useful life of these devices.**

***Index Terms*—Insulated gate bipolar transistors, precursors, prognostics.**

ACRONYM[1]

BJT	bipolar junction transistor
FMMEA	failure modes, mechanisms, and effects analysis
IGBT	insulated gate bipolar transistors
MOSFET	metal oxide semiconductor field effect transistor
PoF	physics of failure
SAM	scanning acoustic microscopy

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Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

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[1]The singular and plural of an acronym are always spelled the same.

I. INTRODUCTION

A FAILURE precursor is an event or series of events indicative of an impending failure [1]. Prognostics is the process of predicting the future health of a product by assessing the extent of deviation or degradation from its expected typical operating conditions [2], and by extrapolating the behavior to damage thresholds using appropriate models and algorithms. These models and algorithms may need to incorporate not only features derived from monitored precursor signals, but also current, and future environmental conditions, and operational loads.

In this paper, precursor parameters are identified for insulated gate bipolar transistors (IGBT). IGBT are used in applications such as the switching of automobile and train traction motors, and in switch mode power supplies (SMPS) to regulate DC voltage. The failure of these switches can reduce the efficiency of the system, or lead to system failure. By implementing prognostics on critical components such as IGBT, cost benefits can be achieved by avoidance of unscheduled maintenance while improving safety.

IGBT have switching characteristics similar to a metal oxide semiconductor field effect transistor (MOSFET), and the high current and voltage capabilities of a bipolar junction transistor (BJT) [3]. The structure of an IGBT is similar to that of a vertical diffusion power MOSFET, except for an additional p+ layer above the collector as seen in Fig. 1. The main characteristic of the vertical configuration is that the collector (drain) forms the bottom of the device while the emitter (source) region remains the same as a traditional MOSFET. Fig. 1 represents the schematic structure of the device used in this study. The additional p+ layer in the IGBT acts as a source of holes that are injected into the body (n- region) during operation. These injected holes enable quick turn-off by recombination with excess electrons that remain in the body of the IGBT after switch-off.

The current flow in this device is composed of both holes, and electrons. Applying a positive voltage to the gate switches on the device when a conductive n-channel, also known as the inversion layer, is created. Electrons flow from the emitter through the conductive n-channel to the collector terminal. A positive voltage applied to the collector with the emitter at ground causes the injection of positive carriers from the p+ layer into the body, which allows for conductivity modulation of the device, leading to a lower on-resistance compared to the power MOSFET. Because an IGBT is switched on by voltage rather than current, it results in faster switching speeds in comparison to BJT. As the conductivity of the device is modulated by charge injection

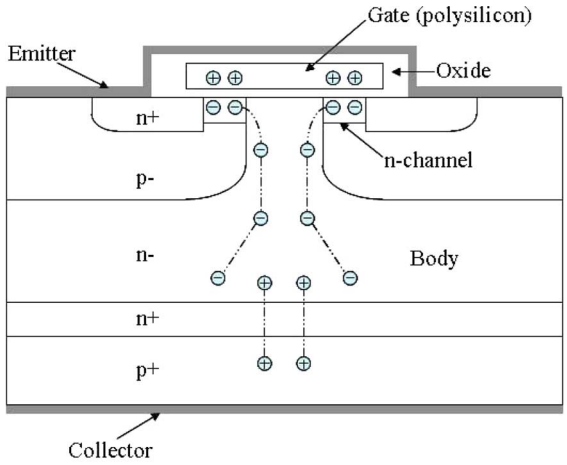

Fig. 1. Schematic of IGBT operation.

from the p+ layer, it allows for lower on-state resistance than the power MOSFET. The punch-through IGBT used in this study has an additional n+ layer, called the buffer layer, above the p+ layer that contacts the collector terminal. The additional n+ layer leads to faster evacuation of stored charges resulting in increased switching speed of the IGBT.

II. Accelerated Aging for IGBT

Failure precursor parameter identification on IGBT has been carried out by performing accelerated aging with in-situ monitoring of selected parameters, followed by electrical, and physical degradation analysis to correlate changes in monitored parameters to degradation in the devices under test. Accelerated aging conditions were based on failure modes, mechanisms, and effects analysis (FMMEA) of IGBT described in [4]. The failure modes for the IGBT include short circuits, increased leakage current, or loss of gate control. The potential failure causes for the failure modes involve high electric fields, and/or high temperatures. In this study, IGBT were subjected to thermal overstress to degrade the parts.

Aging of IGBT in a controlled environment with the purpose to monitor degradation parameters and capture damage propagation characteristics was first realized by Ginart *et al.* [5]. Thermal-electrical stress was used in their work to generate device damage by applying a controlled temperature. The damage was realized by reducing the heat transfer capability of the IGBT (removing the heat sink), then switching the component such that it would heat itself. The IGBT's case temperature was controlled in a feedback loop to ensure a gradual regulation of the aging process. The custom test-bed provided measurements of collector-to-emitter voltage, and current needed to compute the collector-to-emitter resistance. The temperature was measured at the front, and back surfaces of the package. Using a thermal model, the junction temperature was approximated. While this process may not allow accurate measurement or control of the die temperature, it did effectively allow for aging in a repeatable fashion. Gate current, and the gate voltage were measured as well. The findings derived from this testbed include ringing characteristics that can be effectively used as failure precursors [6]. The aging testbed employed to age the devices used in the study presented here uses concepts from the work described by Ginart *et al.* [5], [6], and has been described in Sonnenfeld *et al.* [7]. The overview of the instrumentation and control system used for IGBT aging is shown in Fig. 2. The test hardware consists of an oscilloscope for transient signal acquisition, a function generator for generating gate signals, programmable power supplies, and a data acquisition module.

Thermal overstress tests were conducted on eight International Rectifier IRG4BC30KDPBF IGBT with a 600V/16A current rating using a transistor test board, as shown in Fig. 3.

The safe operating area determines the current and voltage limits within which the IGBT can be operated without destructive failure. For the IGBT under study, the gate voltage limit is 20 V, with the limit on collector-emitter voltage being 600 V, and collector currents limited to below 60 A. The maximum operating junction temperature is 150 °C [8]. For aging the IGBT, the gate voltage was chosen to be a square signal with amplitude of 8 V, a frequency of 1 kHz, and a duty cycle of 40%. The collector-emitter was biased at 4 V. The currents and voltages were maintained within the safe operating area, while the temperature was raised beyond the maximum rating to induce latch-up. The temperature controller was designed to keep the case temperature of the transistor within a hysteresis bound. The square signal voltage was applied to the gate until the upper bound was reached. The gate voltage was then turned off until the temperature dropped to the lower bound. Additionally, a third temperature bound was set to shutdown the power supply to prevent device burn out.

The maximum case temperature attained during the aging was 340 °C. The aging of the device was carried out until loss of gate control was observed. This behavior is indicative of latch-up attributed to the temperature stimulated parasitic thyristor found within the IGBT structure. Latch-up occurs when the parasitic P-N-P-N thyristor structure inherent in the device is activated. On latch-up, the collector current is no longer controlled by the gate. If the bias across the IGBT is not removed when latch-up occurs, the device burns out.

The latch-up time for the transistors varied from 30 minutes to 2 hours. The collector-emitter current, transistor case temperature, transient and steady state gate voltages, and transient and steady state collector-emitter voltages were monitored in-situ during the test.

The transient collector-emitter voltage showed a reduction with increased aging time. The turn-off time for the transistors increased with aging. The turn-off time is a function of the time taken for the transistor to reach the peak value of the collector-emitter voltage. A plot of changes in the transient collector-emitter voltage with aging time is shown for one of the transistors (part B) in Fig. 4. This plot shows an increase in the turn-off time with aging. The observation numbers on the abscissa in Fig. 4 correspond to a time period of 8 ns.

III. Characterization of Aged IGBTs

The IGBT were characterized before, and after the aging tests. The characterization tests included measurements of the threshold voltage, capacitance-voltage (C-V), and I-V plots for low and high gate voltages, collector-emitter ON voltage,

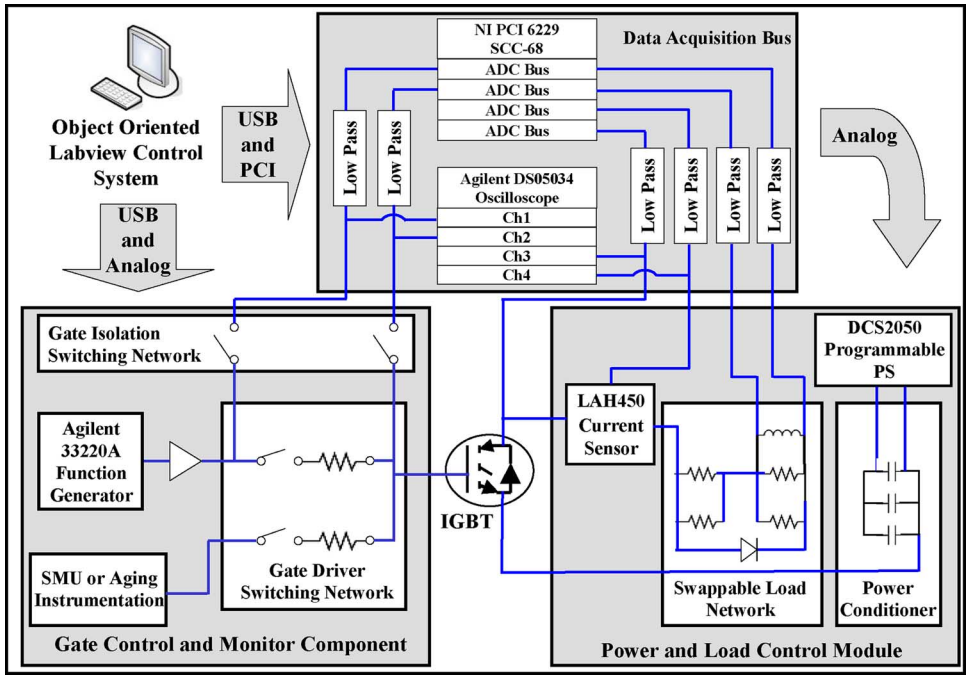

Fig. 2. Overview of the aging and characterization system [7].

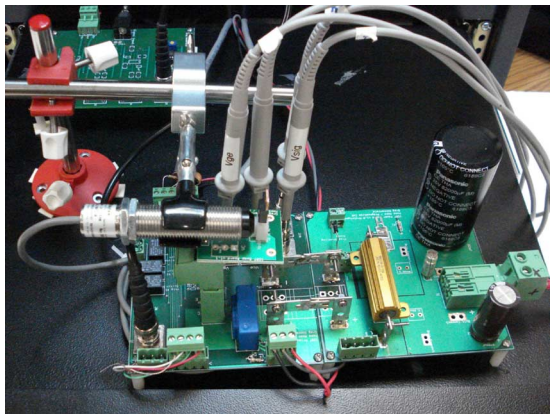

Fig. 3. IGBT aging and characterization test board.

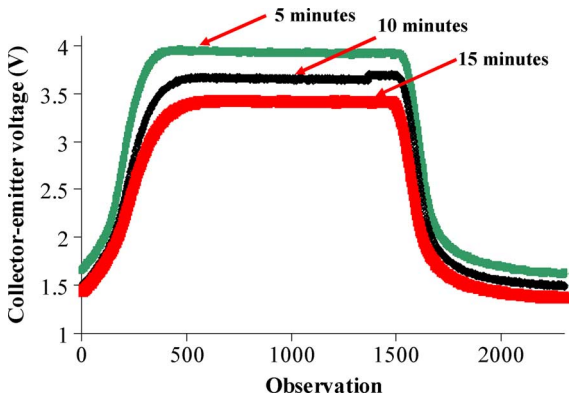

Fig. 4. Transient collector-emitter voltage variation with aging time.

and scanning acoustic microscopy (SAM) analysis. All the characterization tests were performed at room temperature.

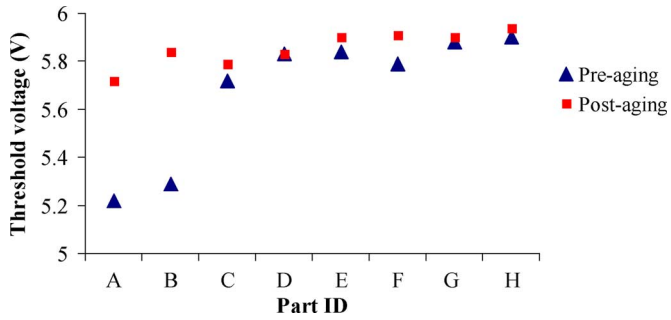

Fig. 5. Threshold voltage variation with aging.

A. *Threshold Voltage*

The threshold voltage is the gate voltage at which the IGBT turns on, and collector current begins to flow. The threshold voltage was measured using an Agilent 4155C semiconductor parameter analyser. Based on the part data-sheet [8], the threshold voltage was measured at a collector current of 250 μA at room temperature. From the pre-, and post-aging characterization, we observed that aging had led to an increase in the threshold voltage of seven of the eight devices tested. The maximum increase in the threshold voltage was 11% for part B, as shown in Fig. 5.

An increase in the threshold voltage is an indicator of gate oxide degradation. The results of threshold voltage measurements were not conclusive as one of the parts (part D) showed no changes with aging. To further assess the degradation in the gate oxide, C-V measurements were performed.

B. *Capacitance-Voltage (C-V) Measurements*

Quasi-static capacitance voltage (QSCV) measurements were performed to verify the nature of trapped charges in the gate

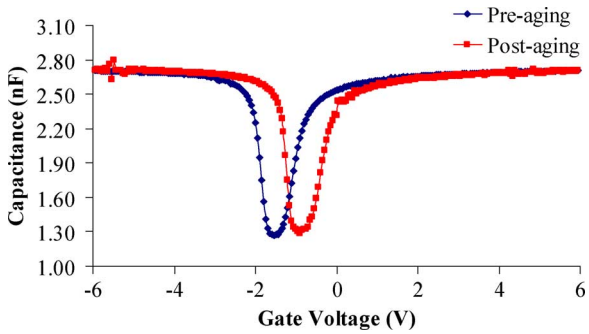

Fig. 6. C-V measurement for part A.

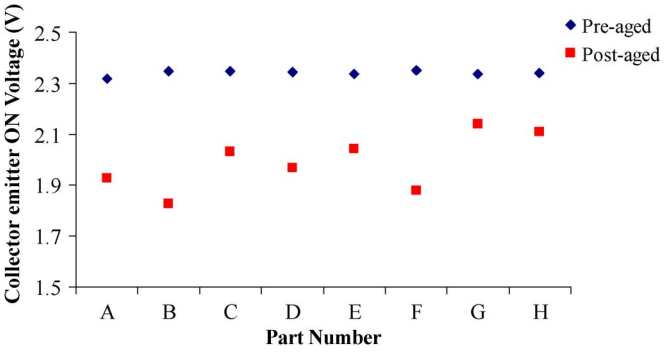

Fig. 7. Collector-emitter ON voltage variation with aging.

oxide of the IGBT [9]. These measurements were performed on the Agilent 4155C semiconductor parameter analyser. The C-V plot for part A is shown in Fig. 6. The gate voltage was swept from −6 V to +6 V, and the capacitance was measured across the gate-emitter terminals.

If charges accumulate in the gate oxide during aging, the C-V plot translates (shifts) along the gate voltage axis. The shape of the plot remains unchanged. The C-V plot translates to the right if the oxide trapped charge is negative, and to the left if the trapped charge is positive [10]. For all the parts, a right shift in the C-V measurements was observed showing the presence of trapped electrons in the gate oxide as a result of aging.

C. Collector-Emitter ON Voltage

The collector-emitter ON voltage was measured across the collector-emitter terminals of the transistor at a collector current of 16 A, and gate voltage of 15 V. The collector-emitter voltage measurements were made in the linear region of the I-V curve. A Tektronix 371A high power curve tracer was used to characterize the IGBT before, and after aging. The results of the characterization are shown in Fig. 7.

From the results, we observe that the collector-emitter ON voltage reduces with aging. There is an increased scatter in the voltage values as a result of variation in the time taken for each transistor to latch-up. The maximum voltage drop of 25% was observed for part B, and the minimum voltage drop was observed for part G. The lowered voltage drop across the transistor with aging indicates reduced effective resistance of the transistor as this parameter is measured at a constant current. The reduction in the effective resistance of the transistors with aging as indicated by the reduction in collector-emitter voltage results

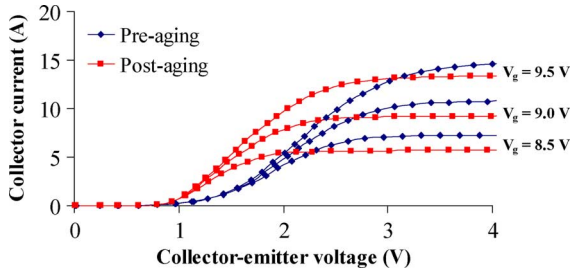

Fig. 8. I-V characteristics of IGBT.

were verified by I-V characterization tests. In the linear region of the I-V curves, the post-aged IGBT were observed to output higher collector current in comparison to pre-aged IGBT. The linear region is defined as the region where the collector current is proportional to the collector-emitter voltage. The higher currents for the aged parts in the linear region indicates reduced effective resistance of the parts with aging. This is shown in Fig. 8, where I-V curves for gate voltages of 8.5 V, 9 V, and 9.5 V are plotted.

D. Scanning Acoustic Microscopy (SAM)

Scanning acoustic microscopy (SAM) is a non-destructive analysis technique that can be used to detect delaminations and voids in microelectronic packages. In this technique, an acoustic transducer emitting a high frequency sound wave scans the package. At various interfaces within the package, part of the incident acoustic energy is reflected, and the rest is transmitted. The reflected signals are sensed by the transducer, and converted back into electrical signals. The electrical signals are then analysed (also referred to as pulse-echo mode analysis), and are used to form images of the internal structures, and defects.

The SAM analysis was performed in this study to determine the effects of aging on the IGBT package. The SAM analysis was conducted on the TO-220 package of the IGBT with the heat-sink facing the transducer. A 35 MHz transducer was used in the pulse-echo mode for the SAM inspections.

A-scans, and C-scans were obtained for the IGBT. A-scan is a time-domain analysis of the reflected acoustic signal. A-scan is performed to focus the microscope, and determine the specific interface within the package to be imaged. C-scan, also called CSAM, provides an image of the interface of interest as determined by the A-scan. The analysis of the A-scan and C-scan images therefore helps identify the site, and degree of degradation. The A-scan images of part F before, and after aging are shown in Fig. 9. The first peak is the reflected signal from the heat-sink, and the second signal is the reflected signal from the die attach. The C-scan image of the die attach of part F before, and after aging is shown in Fig. 10. The device package is called a co-pack as it contains the IGBT (on the right), as well as the free-wheeling diode (on the left), as shown in Fig. 10.

In the C-scan image of the die attach, dark areas denote good adhesion, and are areas where most of the acoustic energy in the acoustic pulse is transmitted. The bright areas in the die attach indicate increased reflection due to degradation [11]. Comparing the brightness of point 2 in Fig. 10 for the pre-, and

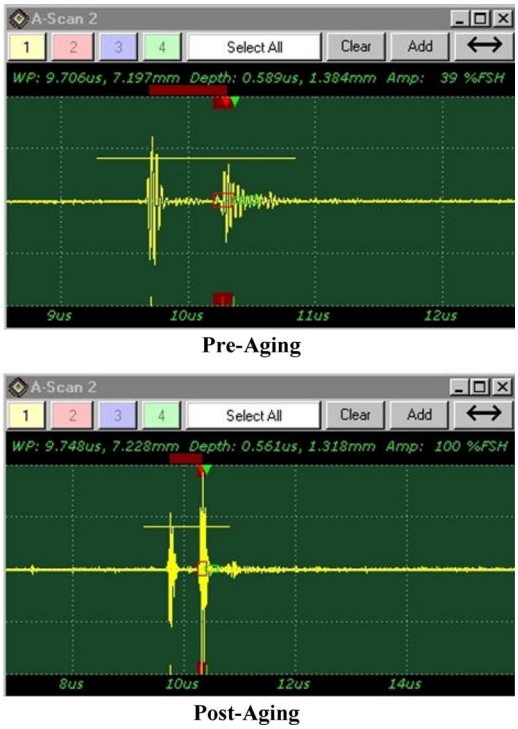

Fig. 9. A-scan of part F.

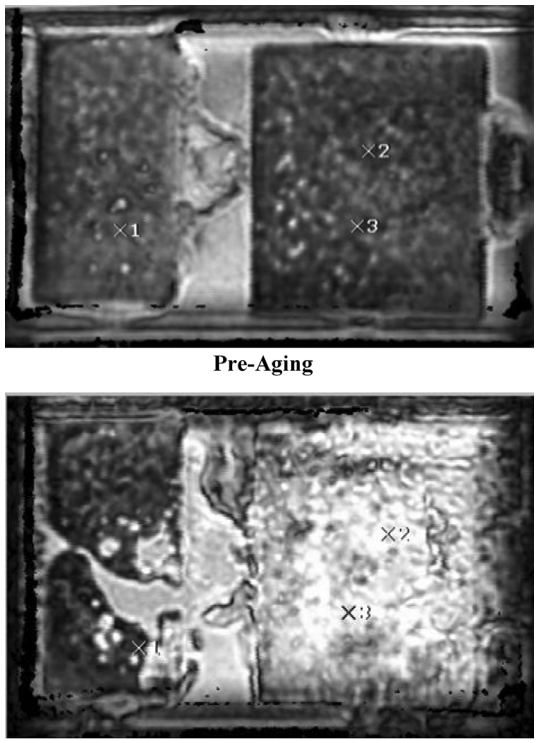

Fig. 10. C-scan of part F.

post-aged part F, it is observed that aging has led to degradation. A significant increase in the amplitude of the reflected signal from the die attach of part F at point 2 is shown in the A-scan in Fig. 9, indicating increased reflection due to degradation.

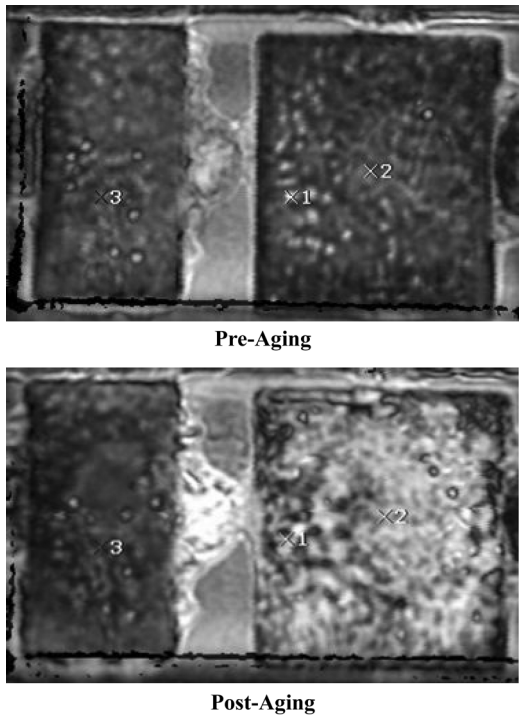

Fig. 11. C-scan of part H.

All the aged parts were observed to have degradation in the die attach. However, there was significant variation observed in the degree of degradation. For example, Part F in Fig. 10 has more die attach degradation in comparison to part H in Fig. 11 after aging.

IV. Discussion, and Conclusions

From the aged IGBT characterization results, it is observed that aging has resulted in gate oxide degradation due to the presence of trapped electrons, as verified by the capacitance-voltage (C-V) plots. The degree of die attach degradation observed in CSAM was found to follow the trend of the reduction in collector-emitter ON voltage after aging for all the eight parts. With increased die attach degradation, increased drop in the collector-emitter ON voltage was observed. An example of this behavior is shown by comparing the plot for the collector-emitter ON voltage in Fig. 7 with the C-scan images shown in Figs. 10 and 11. Part F, which has a more degraded die attach in comparison to part H, also has a greater drop in collector-emitter ON voltage after aging. The die attach is an integral part of the heat dissipation path, and its degradation is hypothesized to be the cause for drop in collector-emitter ON voltage. The degraded die-attach leads to an increased temperature at the p-n junction (Fig. 1) above the collector due to increased thermal impedance. The increased temperature at this junction leads to an increase in the intrinsic carrier concentration, resulting in a lowering of the voltage drop at the junction. This is similar to the reduction in collector-emitter ON voltage observed with increasing temperature reported in [12]. The degraded die-attach also leads to an increase in the transistor turn-off time. This slow turn-off occurs due to the increase in the lifetime of minority carriers injected into the n- region (Fig. 1) of the devices during forward current

conduction [12], caused by increased thermal impedance as a result of the degraded die attach.

The increased device temperature due to the degraded die attach makes the device more susceptible to latch-up [13]. The collector current at which latch-up occurs is called the latching current. This magnitude of the collector current required to induce latch-up reduces with increasing device temperature. Hence, the susceptibility to latch-up is higher at higher device temperatures.

From the discussion above, we conclude that two damage mechanisms are in operation; the oxide damage that affects the capacitance–voltage measurements, and the die-attach degradation which affects the collector-emitter ON voltage and the turn-off time. The collector-emitter voltage and transistor turn-off times are precursor parameters to IGBT failure by latch-up as a result of thermal overstress.

The prognostics methodology for IGBT will involve continuously monitoring the precursor parameters, and comparing their behavior with the baseline developed for healthy devices. This comparison will allow for anomaly detection. The precursor parameters that contribute significantly to the anomalies detected can then be isolated. The isolated parameters will be used to identify relevant physics of failure (PoF) models. Using PoF models, and data-driven techniques for parameter isolation and trending, the remaining useful life of IGBT can be determined. For RUL estimates for IGBT under thermal overstress, continuous monitoring of precursor parameters identified in this study, along with the use of relevant physics of failure (PoF) models for die attach and gate oxide degradation, will enable estimation of remaining useful life.

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